REMARKS

The following remarks are made in response to the Non-Final Office Action mailed January 6, 2005. In that Office Action, the Examiner rejected claims 1, 6-9, 11, 14, and 19 under 35 U.S.C. §102(e) as being anticipated by Crisan, U.S. Patent No. 6,105,140 ("Crisan"). Claims 2, 12, and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Crisan in view of Byers et al., U.S. Patent No. 5,594,893 ("Byers"). Claims 3-5 and 16-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Crisan in view of Han et al., U.S. Patent No. 5,989,043 ("Han"). Claims 10, 13, and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Crisan in view of Ten Holter, U.S. Patent No. 6,351,083 ("Ten Holter").

With this Response, Applicant respectfully traverses the Examiner's rejection of claims 1-20. Claims 1-20 remain pending in the application and are presented for reconsideration and allowance.

35 U.S.C. §102 Rejections

The Examiner rejected claims 1, 6-9, 11, 14, and 19 under 35 U.S.C. §102(e) as being anticipated by Crisan, U.S. Patent No. 6,105,140 ("Crisan"). Independent claim 1 is directed to "a host processor card configured to be fitted into a server system", and recites "a graceful shutdown circuit coupled to the processor and the power control line, the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit, the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal." The Examiner indicated that Crisan discloses a graceful shutdown circuit as recited in claim 1 at column 6, lines 16-20 and lines 60-67, and at column 7, lines 1-8. (Office Action at para. no. 3, page 3). These portions of Crisan disclose that:

> In the system S of FIG. 1, all electronic devices discussed above, including the processors, are powered by a regulated power supply 170, as shown in FIGS. 14. The regulated power supply 170 (FIG. 2) has a security control interface circuitry connected to the primary PCI bus 117 (FIGS. 1 and 2). (Crisan at col. 6, lines 16-20).
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> . . .

> Thus, the switch 165 normally provides an electrical connection for the AC voltage from the plug 166 to the power supply 170. The decoder 164, upon receipt of a shutdown instruction sent by the processor in response to the interrupt signal from the interrupt controller 124, passes the shutdown instruction in the form of an actuation signal to the switch 165. The assertion of the actuation signal causes the switch 165, which could be electronic or electromechanical, including power FETs, relays or solid state relays, to be actuated so as to break or to complete the electrical connection between the plug 166 and the power supply 170. Thus, upon receipt of the shutdown command by the processor after someone toggles the power supply on/off switch 162 and after the proper password has been entered, the switch 165 disables the power supply 170 so that the system can be safely powered down. (Crisan at col. 6, line 60, to column 7, line 8).

The above-quoted portions relate to Figure 2 of Crisan, which shows a first embodiment of a "secure power supply" of the computer system S shown in Figure 1. (See, e.g., Crisan at col. 3, lines 6-12; col. 6, lines 16-21; and col. 7, lines 9-10). In contrast, claim 1 is directed to "a host processor card", not a power supply. There is no teaching or suggestion in these cited portions of Crisan that processor card C (Figure 1 of Crisan) includes a graceful shutdown circuit, let alone "a graceful shutdown circuit coupled to the processor and the power control line, the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit, the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal", as recited in claim 1.

In view of the above, Crisan does not teach or suggest each and every limitation of independent claim 1. Applicant respectfully requests removal of the rejection of claim 1 under 35 U.S.C. § 102(e), and requests allowance of this claim. Since dependent claims 6-9 further limit patentably distinct claim 1, claims 6-9 are believed to be allowable over the cited reference, and allowance of claims 6-9 is respectfully requested.

Independent claim 11 is directed to "a graceful shutdown circuit for a host processor card". As described above with respect to independent claim 1, Crisan discloses a "secure power supply", and does not teach or suggest a host processor card with a graceful shutdown circuit as recited in claim 1. For the reasons described above with respect to claim 1, Crisan

also does not teach or suggest a graceful shutdown circuit for a host processor card as recited in independent claim 11. In addition, claim 11 recites "a first input configured to be coupled to a processor of the host processor card, the first input indicating whether a graceful shutdown is to be performed". The Examiner indicated that this limitation was disclosed at column 7, lines 54-58, and col. 8, lines 4-8, of Crisan. (Office Action at para. no. 8, page 4). These portions of Crisan disclose that:

> The interrupt approach is more efficient because it allows the processor to execute its main program and to service peripheral devices such as the on-off switch 162 only when requested by the device itself. (Crisan at col. 7, lines 54-58).
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> . . .
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> On receipt of the interrupt signal such as the signal from the power supply on/off switch 162, the interrupt controller 124 pulses the interrupt input of the processor. The processor completes the currently executing instruction, issues an interrupt acknowledge signal to the PIC 124 and then executes a service routine to service the requesting device. (Crisan at col. 8, lines 3-8).

The above-quoted portion of Crisan indicates that the processor of the computer system S of Crisan includes an interrupt input. This cited portion of Crisan does not teach or suggest an input of a graceful shutdown circuit, that the input of the graceful shutdown circuit is configured to be coupled to a processor of a host processor card, or that the input indicates to the graceful shutdown circuit that a graceful shutdown is to be performed.

In view of the above, Crisan does not teach or suggest each and every limitation of independent claim 11. Applicant respectfully requests removal of the rejection of claim 11 under 35 U.S.C. § 102(e), and requests allowance of this claim.

Independent claim 14 is directed to "a method of gracefully shutting down a host processor card in a server system", and recites "providing a graceful shutdown indication from an operating system of the host processor card to a processor of the host processor card when an immediate shutdown of the host processor card should not be performed". The Examiner indicated that this limitation was disclosed at column 9, lines 25-34, and col. 10, lines 43-51, of Crisan. (Office Action at para. no. 9, page 5). These portions of Crisan disclose that:

> Next, in step 204, the system checks to see if a power-off key or password has been entered. If not, in step 206, the system requests the user to enter a

> selected password as the power-off key. In step 208, the entered power-off key is stored in the flash ROM 154, or alternatively in the non-volatile RAM 152. From step 208, or from step 204 if the power off key has been entered already, the system S continues its booting process in step 210. (Crisan at col. 9, lines 25-34).
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> At this step, normal operation cannot continue until the power switch 162 is turned on again or until the correct password has been entered. From step 284, the routine checks the validity of the password in step 286. If the password matches the key, the routine initiates the operating system shutdown in step 290. This will ensure that the cache is cleared and that the operating system is shut down properly. From step 290, a register is set to indicate that the system that power is to be turned off instead of the initiation of the POST (Power On Self-Test) operations in step 290. (Crisan at col. 10, lines 43-51).

The above-quoted portion of Crisan indicates that an operating system shutdown is initiated if a correct password is entered by a user. If the correct password is entered, the operating system is shut down, and if the correct password is not entered, the operating system is not shut down. This cited portion of Crisan does not teach or suggest anything regarding a graceful shutdown versus an immediate shutdown, or that the operating system provides a graceful shutdown indication to a processor of a host processor card when an immediate shutdown of the host processor card should not be performed.

Independent claim 14 also recites "outputting a graceful shutdown signal from the processor when an immediate shutdown of the host processor card should not be performed". The Examiner indicated that this limitation was disclosed at column 7, lines 54-58, and col. 8, lines 4-8, of Crisan. (Office Action at para. no. 9, page 5). These portions of Crisan disclose that:

> The interrupt approach is more efficient because it allows the processor to execute its main program and to service peripheral devices such as the on-off switch 162 only when requested by the device itself. (Crisan at col. 7, lines 54-58).
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> . . .
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> On receipt of the interrupt signal such as the signal from the power supply on/off switch 162, the interrupt controller 124 pulses the interrupt input of the processor. The processor completes the currently executing instruction, issues an interrupt acknowledge signal to the PIC 124 and then executes a service routine to service the requesting device. (Crisan at col. 8, lines 3-8).

The above-quoted portion of Crisan indicates that the processor of the computer system S of Crisan includes an interrupt input. This cited portion of Crisan does not teach or suggest anything regarding a graceful shutdown versus an immediate shutdown, or that the processor outputs a graceful shutdown signal when an immediate shutdown of a host processor card should not be performed.

In view of the above, Crisan does not teach or suggest each and every limitation of independent claim 14. Applicant respectfully requests removal of the rejection of claim 14 under 35 U.S.C. § 102(e), and requests allowance of this claim. Since dependent claim 19 further limits patentably distinct claim 14, claim 19 is believed to be allowable over the cited reference, and allowance of claim 19 is respectfully requested.

35 U.S.C. §103 Rejections

The Examiner rejected claims 2, 12, and 15 under 35 U.S.C. §103(a) as being unpatentable over Crisan in view of Byers et al., U.S. Patent No. 5,594,893 ("Byers"). Dependent claim 2 is dependent on independent claim 1. As described above with respect to claim 1, Crisan does not teach or suggest a host processor card with "a graceful shutdown circuit coupled to the processor and the power control line, the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit, the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal", as recited in claim 1. Byers also does not teach or suggest this limitation of claim 1. Since dependent claim 2 further limits patentably distinct claim 1, claim 2 is believed to be allowable over the cited references, and allowance of claim 2 is respectfully requested.

Dependent claim 12 is dependent on independent claim 11. As described above with respect to claim 11, Crisan does not teach or suggest a graceful shutdown circuit for a host processor card, and Crisan does not teach or suggest "a first input configured to be coupled to a processor of the host processor card, the first input indicating whether a graceful shutdown is to be performed", as recited in claim 11. Byers also does not teach or suggest this limitation of claim 11. Since dependent claim 12 further limits patentably distinct claim 11,

claim 12 is believed to be allowable over the cited references, and allowance of claim 12 is respectfully requested.

Dependent claim 15 is dependent on independent claim 14. As described above with respect to claim 14, Crisan does not teach or suggest "providing a graceful shutdown indication from an operating system of the host processor card to a processor of the host processor card when an immediate shutdown of the host processor card should not be performed", or "outputting a graceful shutdown signal from the processor when an immediate shutdown of the host processor card should not be performed", as recited in claim 14. Byers also does not teach or suggest these limitations of claim 14. Since dependent claim 15 further limits patentably distinct claim 14, claim 15 is believed to be allowable over the cited references, and allowance of claim 15 is respectfully requested.

The Examiner rejected claims 3-5 and 16-18 under 35 U.S.C. §103(a) as being unpatentable over Crisan in view of Han et al., U.S. Patent No. 5,989,043 ("Han"). Dependent claims 3-5 are dependent on independent claim 1. As described above with respect to claim 1, Crisan does not teach or suggest a host processor card with "a graceful shutdown circuit coupled to the processor and the power control line, the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit, the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal", as recited in claim 1. Han also does not teach or suggest this limitation of claim 1. Since dependent claims 3-5 further limit patentably distinct claim 1, claims 3-5 are believed to be allowable over the cited references, and allowance of claims 3-5 is respectfully requested.

Dependent claims 16-18 are dependent on independent claim 14. As described above with respect to claim 14, Crisan does not teach or suggest "providing a graceful shutdown indication from an operating system of the host processor card to a processor of the host processor card when an immediate shutdown of the host processor card should not be performed", or "outputting a graceful shutdown signal from the processor when an immediate shutdown of the host processor card should not be performed", as recited in claim 14. Han also does not teach or suggest these limitations of claim 14. Since dependent claims 16-18

further limit patentably distinct claim 14, claims 16-18 are believed to be allowable over the cited references, and allowance of claims 16-18 is respectfully requested.

The Examiner rejected claims 10, 13, and 20 under 35 U.S.C. §103(a) as being unpatentable over Crisan in view of Ten Holter, U.S. Patent No. 6,351,083 ("Ten Holter"). Dependent claim 10 is dependent on independent claim 1. As described above with respect to claim 1, Crisan does not teach or suggest a host processor card with "a graceful shutdown circuit coupled to the processor and the power control line, the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit, the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal", as recited in claim 1. Ten Holter also does not teach or suggest this limitation of claim 1. Since dependent claim 10 further limits patentably distinct claim 1, claim 10 is believed to be allowable over the cited references, and allowance of claim 10 is respectfully requested.

Dependent claim 13 is dependent on independent claim 11. As described above with respect to claim 11, Crisan does not teach or suggest a graceful shutdown circuit for a host processor card, and Crisan does not teach or suggest "a first input configured to be coupled to a processor of the host processor card, the first input indicating whether a graceful shutdown is to be performed", as recited in claim 11. Ten Holter also does not teach or suggest this limitation of claim 11. Since dependent claim 13 further limits patentably distinct claim 11, claim 13 is believed to be allowable over the cited references, and allowance of claim 13 is respectfully requested.

Dependent claim 20 is dependent on independent claim 14. As described above with respect to claim 14, Crisan does not teach or suggest "providing a graceful shutdown indication from an operating system of the host processor card to a processor of the host processor card when an immediate shutdown of the host processor card should not be performed", or "outputting a graceful shutdown signal from the processor when an immediate shutdown of the host processor card should not be performed", as recited in claim 14. Ten Holter also does not teach or suggest these limitations of claim 14. Since dependent claim 20 further limits patentably distinct claim 14, claim 20 is believed to be allowable over the cited

references, and allowance of claim 20 is respectfully requested.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-20 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-20 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either David M. Mason at Telephone No. (408) 447-4046, Facsimile No. (408) 447-0854 or Jeff A. Holmen at Telephone No. (612) 573-0178, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 17th day of **March**, **2005**.

By

Name: **Jeff A. Holmen**